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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
MASKULINSKI, MICHAEL C	
ART UNIT	**PAPER NUMBER**
2113	

DATE MAILED: 02/02/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/716,984	DRISCOLL, KEVIN RAYMOND	
	Examiner	Art Unit	
	Michael C. Maskulinski	2113	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 November 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-6,9-19 and 22-26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,10,12-14,23,25 and 26* is/are rejected.

7)☒ Claim(s) *2-6,9,11,15-19,22 and 24* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *18 November 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Non-Final Office Action

Double Patenting

1. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory obviousness-type double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., In re Berg, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); In re Goodman, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); In re Longi, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); In re Van Ornum, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); In re Vogel, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and In re Thorington, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent either is shown to be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement.

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

2. Claims 1-6, 9-19, and 22-26 are rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 1-5, 8-12, 14-18, 20-24 of U.S. Patent No. 6,678,836 B2. Although the conflicting claims are not identical, they are not patentably distinct from each other because of the following.

Referring to claim 1, claims 1 and 7 of U.S. Patent 6,678,836 B2 disclose a method for remapping locations in memory, comprising: generating a remapping value by logically combining a bad address value with an unused address value; logically combining the remapping value with an intended address value to generate a remapped address value, wherein one or more bad memory address values exist and wherein the

remapping value is logically combined with only intended address values that equal one of the bad memory address values to generate a remapped address value for only the one or more bad memory address values; and accessing a memory location having the remapped address value.

Although the conflicting claims are not identical, they are not patentably distinct from each other because claims 1 and 7 of U.S. Patent 6,678,836 B2 include all of the limitations in claim 1 of the instant application. With regard to the additional limitations in claims 1 and 7 of U.S. Patent 6,678,836 B2, which are not included in claim 1 of the instant application, the omission of these limitations in claim 1 of the instant application is an obvious expedient since the remaining limitations in claims 1 and 7 of U.S. Patent 6,678,836 B2 perform the same function as the limitations in claim 1 of the instant application (*In re Karlson*, 136 USPQ 184 (CCPA 1963)).

Referring to claim 2, claim 1 of U.S. Patent 6,678,836 B2 discloses generating a remapping value by logically combining a bad address value with an unused address value.

Referring to claim 3, claim 2 of U.S. Patent 6,678,836 B2 discloses wherein the bad memory address value, unused memory address value, and the remapped address value correspond to individual data locations.

Referring to claim 4, claim 3 of U.S. Patent 6,678,836 B2 discloses wherein the bad memory address value and the unused memory address value each correspond to multiple data locations.

Referring to claim 5, claim 4 of U.S. Patent 6,678,836 B2 discloses wherein the bad memory address value, unused memory address value, and the remapped address value correspond to individual memory pages.

Referring to claim 6, claim 5 of U.S. Patent 6,678,836 B2 discloses wherein the bad memory address value and the unused memory address value each correspond to multiple memory pages.

Referring to claim 9, claim 8 of U.S. Patent 6,678,836 B2 discloses wherein the bad memory address value and the unused memory address value are exclusively-ORed to produce the remapping value.

Referring to claim 10, claim 9 of U.S. Patent 6,678,836 B2 discloses wherein the remapping value and the intended address value are exclusively-ORed to produce the remapped address value.

Referring to claim 11, claim 10 of U.S. Patent 6,678,836 B2 discloses wherein the bad memory address value and the unused memory address value are exclusively-NORed to produce the remapping value.

Referring to claim 12, claim 11 of U.S. Patent 6,678,836 B2 discloses wherein the remapping value and the intended address value are exclusively-NORed to produce the remapped address value.

Referring to claim 13, claim 12 of U.S. Patent 6,678,836 B2 discloses wherein the remapping value is latched.

Referring to claim 14, claims 13 and 19 of U.S. Patent 6,678,836 B2 discloses a system for remapping locations in memory, comprising: a first logic for outputting a

remapping value by logically combining a bad memory address value with an unused memory address value; a second logic configured to combine the remapping value with an intended address value to generate a remapped address value, wherein the second logic combines the remapping value with only the intended address value that equals the bad memory address value to generate a remapped address value for only the bad memory address value and a memory address input configured to access a memory location having the remapped address value.

Although the conflicting claims are not identical, they are not patentably distinct from each other because claims 13 and 19 of U.S. Patent 6,678,836 B2 includes all of the limitations in claim 14 of the instant application. With regard to the additional limitations in claims 13 and 19 of U.S. Patent 6,678,836 B2, which are not included in claim 14 of the instant application, the omission of these limitations in claim 14 of the instant application is an obvious expedient since the remaining limitations in claims 13 and 19 of U.S. Patent 6,678,836 B2 perform the same function as the limitations in claim 14 of the instant application (*In re Karlson*, 136 USPQ 184 (CCPA 1963)).

Referring to claim 15, claim 13 of U.S. Patent 6,678,836 B2 discloses a first logic for outputting a remapping value by logically combining a bad memory address value with an unused memory address value.

Referring to claim 16, claim 14 of U.S. Patent 6,678,836 B2 discloses wherein the bad memory address value, unused memory address value, and the remapped address value correspond to individual data locations.

Referring to claim 17, claim 15 of U.S. Patent 6,678,836 B2 discloses wherein the bad memory address value and the unused memory address value each correspond to multiple data locations.

Referring to claim 18, claim 16 of U.S. Patent 6,678,836 B2 discloses wherein the bad memory address value, unused memory address value, and the remapped address value correspond to individual memory pages.

Referring to claim 19, claim 17 of U.S. Patent 6,678,836 B2 discloses wherein the bad memory address value and the unused memory address value each correspond to multiple memory pages.

Referring to claim 22, claim 20 of U.S. Patent 6,678,836 B2 discloses wherein the first logic is an exclusive OR gate.

Referring to claim 23, claim 21 of U.S. Patent 6,678,836 B2 discloses wherein the second logic is an exclusive OR gate.

Referring to claim 24, claim 22 of U.S. Patent 6,678,836 B2 discloses wherein the first logic is an exclusive NOR gate.

Referring to claim 25, claim 23 of U.S. Patent 6,678,836 B2 discloses wherein the second logic is an exclusive NOR gate.

Referring to claim 26, claim 24 of U.S. Patent 6,678,836 B2 discloses further comprising a latch configured to store the remapping value.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1, 10, 13, 14, 23, and 26 are rejected under 35 U.S.C. 102(b) as being anticipated by Doucer, U.S. Patent 5,838,893.

Referring to claims 1 and 14:

a. In column 2, line 67 continued in column 3, lines 1-3, Doucer discloses that the system generates a remapping value that when applied to the addresses in the range remaps the range of bad addresses to the highest possible addresses (generating a remapping value).

b. In column 3, lines 3-6, Doucer discloses that when the system receives an address to use in accessing memory, the system generates a remapped address by applying the remapping value to the received address (logically combining the remapping value with an intended address value to generate a remapped address value, wherein one or more bad memory address values exist and wherein the remapping value is logically combined with only intended address values that equal one of the bad memory address values to generate a remapped address value for only the one or more bad memory address values).

c. In column 3, lines 6-7, Doucer discloses that the system then accesses memory using the remapped address (accessing a memory location having the remapped address value).

Referring to claims 10 and 23, in column 3, lines 24-27, Doucer discloses that the system applies the remapping value to the received address by performing a bitwise

exclusive-OR of the bits of the received address with the bits of the remapping value (wherein the remapping value and the intended address value are exclusively-Ored to produce the remapped address value).

Referring to claims 13 and 26, in column 4, lines 63-65, Doucer discloses that the remapping value is stored in a register. A register inherently is made of at least one latch, therefore, Doucer teaches latching the remapping value.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 12 and 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Doucer, U.S. Patent 5,838,893 as applied to claims 1 and 14 above, and further in view of Logic and Computer Design, by Mano et al.

Referring to claims 12 and 25, in column 3, lines 24-27, Doucer discloses that the system applies the remapping value to the received address by performing a bitwise exclusive-OR of the bits of the received address with the bits of the remapping value. However, Doucer doesn't explicitly disclose using an exclusive-NOR to reproduce the remapping address value. On page 75, Mano et al. disclose that the exclusive-NOR is the complement of the exclusive-OR. It would have been obvious to one of ordinary skill at the time of the invention to include the exclusive-NOR of Mano et al. into the

system of Doucer. A person of ordinary skill in the art would have been motivated to make the modification because an XOR and XNOR gate can be used interchangeably since one is just the complement of the other (see Mano et al.: page 78). Therefore, it is a matter of design choice as to which one is used.

Allowable Subject Matter

7. Claims 2-6, 9, 11, 15-19, 22, and 24 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Response to Arguments

8. Applicant's arguments filed November 18, 2003 have been fully considered but they are not persuasive.

9. On page 1, the Applicant argues, "the '893 patent fails to teach that the remapping value is only combined with bad address values but instead describes applying the remapping value to all address values. This is evident from the specification and FIG. 5 of the '893 patent which shows page 0 being remapped to page 10 even though the bad page is page 5, which is remapped to page 15." The Examiner respectfully disagrees. The Examiner could not find in the specification where pages 0 and 10 are good pages. Instead, in column 4, lines 46-55, the Examiner found that Doucer teaches remapping of bad addresses by combining them with a remapping value. This clearly teaches the claimed limitation.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael C. Maskulinski whose telephone number is (571) 272-3649. The examiner can normally be reached on Monday-Friday 9:30-6:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert W. Beausoliel can be reached on (571) 272-3645. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Michael C Maskulinski
Examiner
Art Unit 2113